AMENDMENTS

In the Specification:

On Page 1, after the title, please replace the first paragraph of the specification, namely "This is a continuation of application no. 09/507,303, filed February 18, 2000" with the following paragraph:

> This application is a continuation of U.S. Application No. 09/507,303, filed 02/18/2000, now U.S. Patent No. 6,266,730, which is a continuation of U.S. Patent Application No. 08/938,084, filed 09/26/1997, now U.S. Patent No. 6,067,594.

In the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1-45. (Previously Cancelled)

46. (Previously Presented) A memory module, comprising:

a first circuit board including a first conductive trace disposed on a surface of the first circuit board;

a first connector including at least one contact connected to the first conductive trace, wherein the first connector is for removably connecting the first circuit board to a second circuit board; and

a first capacitor including:

one capacitor electrode connected to the first connector at a junction where the contact connects to the first conductive trace; and

another capacitor electrode coupled to a node that is at a supply potential.

47. (Previously Presented) The memory module of claim 46, wherein the first connector includes at least one set of edge contacts disposed on the surface.

48. (Previously Presented) The memory module of claim 47, wherein the first connector includes an additional set of edge contacts on another surface substantially parallel to the surface.

49. (Previously Presented) The memory module of claim 46, wherein the contact is a conductive pad disposed on the surface and proximate to an edge of the surface of the first circuit board.

50. (Previously Presented) The memory module of claim 46, wherein the contact is a pin and the first connector comprises a socket for accepting insertion of the second circuit board.

51. (Previously Presented) The memory module of claim 46, wherein the first circuit board is a motherboard and the second circuit board is a daughter board.

52. (Previously Presented) The memory module of claim 46, wherein one of the capacitor electrodes is a conductive pad disposed on the surface of the first circuit board.

53. (Previously Presented) The memory module of claim 46, wherein the supply potential is a ground potential.

54. (Previously Presented) The memory module of claim 46, further comprising a conductive plane disposed parallel to and beneath the surface of the first circuit board, the conductive plane being at a ground potential.

55. (Previously Presented) The memory module of claim 54, further comprising a dielectric disposed between the first conductive trace and the conductive plane.

56. (Previously Presented) The memory module of claim 46, wherein the contact has a first impedance value and the first conductive trace has a second impedance value, wherein the first impedance value is different than the second impedance value.

57. (Previously Presented) The memory module of claim 56, wherein the first capacitor reduces the difference between the first impedance value and the second impedance value.

58. (Previously Presented) The memory module of claim 46, further comprises a plurality of memory devices coupled to the first conductive trace.

59. (Previously Presented) The memory module of claim 46, wherein the first conductive trace comprises a microstrip.

60. (Previously Presented) The memory module of claim 46, wherein a width of a first segment of the first conductive trace is varied with respect to a width of a second segment of the first conductive trace.

61. (Previously Presented) The memory module of claim 60, wherein the width of the first segment is varied with respect to the width of the second segment to reduce a difference

between an impedance value of the first segment and an impedance value of the second segment.

62. (Previously Presented) The memory module of claim 46, further comprising:

the second circuit board;

a second conductive trace disposed on a surface of the second circuit board;

a second connector coupled to the second conductive trace, wherein the second connector mates with the first connector and electrically couples the second conductive trace to the first conductive trace;

a second capacitor including:

one capacitor electrode connected at a junction where the second connector connects to the second conductive trace; and

another capacitor electrode coupled to a node that is at the supply potential.

63. (Previously Presented) The memory module of claim 62, wherein the first circuit board is a motherboard and the second circuit board is a daughter board.

64. (Previously Presented) The memory module of claim 63, wherein a surface of the second circuit board is positioned substantially orthogonal to a surface of the first circuit board.

65. (Previously Presented) The memory module of claim 62, wherein the second capacitor reduces a difference between an impedance value of the second conductive trace and an effective impedance value resulting from the first connector mating with the second connector.

66. (Previously Presented) The memory module of claim 62, wherein the second connector comprises a conductive pad disposed on the surface and proximate to an edge of the second circuit board.

67. (Previously Presented) The memory module of claim 62, wherein the second conductive trace has a right angle turn at each end of the second conductive trace